REMARKS/ARGUMENTS

Claims 1-7 have been amended and claims 8-37 have been added. Thus, claims 1-37 are pending.

Claims 1-7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (USP 3,778,887).

As amended, all the pending claims of the subject application comply with all requirements of 35 U.S.C. Accordingly, Applicant requests examination and allowance of all pending claims.

Summary of Examiner Interview on July 16, 2004:

Applicants thank Examiner Zarneke for the time he spent discussing this case in person on July 16, 2004. During the interview Applicants explained that the holes 23 in the Suziki et al. reference relied upon by Examiner Cruz in the current rejection are positioning holes and are thus not added to the reduce stress. Applicants and the Examiner also discussed a proposed amendment to claim 1 to more particularly claims an embodiment of the invention as well as three new independent claims that are presented herein as claims 9, 21 and 32.

During the interview the Examiner showed Applicants four prior art references including U.S. Patents 4,625,227; 5,773,878; 5,811,874 and 6,075,283 (Applicants have not included these references in an Information Disclosure Statement since it is clear the Examiner is already aware of the references). Applicants briefly reviewed the references and differences between the references and the claims were discussed. In addition to what was discussed during the interview, Applicants would like to point out that the guard ring discussed in USP 4,625,227 and 5,811,874 is formed on the semiconductor chip and not on the lead frame (see e.g., '277 Fig. 5 showing guard ring 12 formed over insulating film 18 on chip 101 and Fig. 3 which shows chip 101 being placed on die pad 9 of the package 8; see also '874, col. 4, line 66 to col. 5, line 2 discussing the guard ring being formed "along peripheral edges of the chip"). Also, with respect to the '878 patent, slits 27 are positioned on a frame that surrounds a single integrated circuit die as compared to a plurality of integrated circuit areas as recited in claim 1.

The Rejection Under 35 U.S.C. § 102

Claims 1-7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (USP 3,778,887). This rejection is respectfully traversed.

As noted in the above Interview Summary, holes 23 in the Suzuki reference are positioning holes (see e.g., col. 4, lines 39-41) and are thus not added to reduce stress. Additionally, claim 1 has been amended to recite the inclusion of a plurality of elongated stress relief openings along each of the four support bars that surround the plurality of integrated circuit areas. The Suziki et al. reference clearly does not teach or suggest this feature of the invention of claim 1.

New Claims

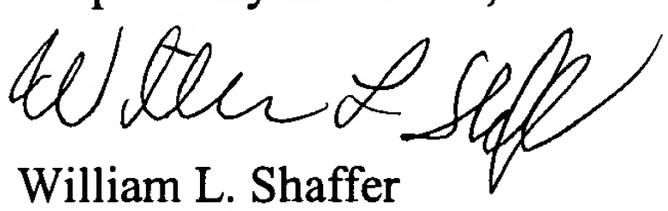
New claims 8-37 have been added to secure an appropriate scope of protection for the present invention. Applicants respectfully request Examination of the new claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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